REMARKS

Applicants appreciate the examination of the present application that is evidenced by the Official Action of February 13, 2008. In response to the Official Action, Applicants have amended Claims 1, 12, 19, 25-27 and 34. In particular, Claims 25-26 have been amended to address the section 112 rejections. Claims 1, 12, 19, 25, 27 and 34 have also been amended to highlight aspects of the invention that are nowhere disclosed or suggested by the cited prior art references, as will now be explained.

Claims 1, 12, 19, 25, 27 and 34 are Patentable Over the Cited Prior Art

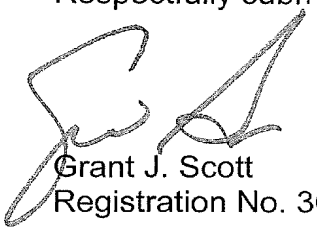
The Official Action acknowledges that Brown does not disclose a control system that is configured to migrate data in response to the indication. However, to provide the missing teaching, the Official Action argues that Hughes et al. discloses a control system "configured to migrate data ... in response to the indication." (Official Action, p. 4). To support this assertion, the Official Action cites FIG. 5 and Col. 10, lines 49-67 of Hughes. But, these portions of Hughes et al. merely disclose circuitry for comparing "expected data" to previously written test data (1 or 0) to determine the location of errors within one or more memory arrays. This data comparison is provided by XOR circuits **505-506**, which merely perform a bit-by-bit comparison between expected data (i.e., the original test data) and the corresponding "test" data read from the memory array(s). According to Hughes et al., if an error is present within the data read from the memory array(s), then a corresponding counter **507-508** is incremented and the corresponding column (or row) of memory containing the defective memory cell is removed from the write/read path of the memory array. (Hughes et al., Col. 10, line 49 - Col. 11, line 39).

Applicants submit that nowhere does Hughes et al. disclose the preservation of actual data (not test data) using a migration operation that occurs in response to the indication. Applicants acknowledge that Hughes et al. discloses a BIST/BISR operation to detect the presence of defective memory cells using test

data, but Hughes et al. provides absolutely no disclosure or suggestion of preserving data using a data migration operation. This omission from Hughes et al. is understandable because the BIST/BISR operations described by Hughes et al. are merely using test data for purposes of preliminary error checking before a memory array(s) is used for storing valuable data.

Thus, notwithstanding the combination of Brown and Hughes et al., Applicants submit that all pending claims are patentable over the cited prior art for at least the reasons that all of the independent claims are patentable.

Respectfully submitted,



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CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on May 13, 2008.

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